Remarks

The final Office Action dated September 16, 2005 has been received and its contents carefully noted. Claims 1-13 are pending in the application. The Examiner rejects claims 1-13 under 35 U.S.C. §102(b) as being anticipated by the Craninckx et al. IEEE Journal Publication that was cited by the Applicant in the Information Disclosure Statement. Claims 5-6 and 13 are objected to for the informalities listed at paragraph 2 on pages 2-3 of the Office Action.

In response thereto, Applicant has amended some of the existing claims in an effort to place the application in condition for allowance. Reconsideration of the objection and rejections of the claims is respectfully requested. The following comments are offered on the cited prior art and it is trusted that they will be persuasive in bringing about a favorable reconsideration and allowance of the claims of the application.

Claim Objections

Claims 5-6 and 13 have been amended to correct the informalities noted by the Examiner. As corrected, Applicant submits that the claim objections are overcome and respectfully requests withdrawal of the claim objections.

Examiner's Response to Arguments/Remarks

Applicant brings to the attention of the Examiner that a Master Slave (M/S) D flip-flop such as disclosed in Craninckx is not the same or equivalent to a polyphase filter as disclosed and claimed in Applicant's application. The M/S half speed circuit of Craninckx divides the input signal by two whereas in Applicant's application the

polyphase filter output signal frequency is the same as the input signal frequency. It is an inherent property of the polyphase filter that frequency of the output signal is the same as the frequency of the input signal. This property and characteristic of a polyphase filter is well known to those skilled in the art. A polyphase filter as used can be seen for example in U.S. Patent Nos. 6,346,850 and 6,480,535.

The frequency of the output signal in the M/S half speed circuit means of Craninckx is one half the frequency of the input signal and therefore the 90° phase difference signal of Craninckx is at a different frequency than the frequency of the input whereas the frequency of the output signals of the polyphase filter are at the same frequency as the input signal. The performance of a fractional multi-modulus prescaler utilizing the M/S half speed circuit means of Craninckx would perform in a totally different manner, if at all, than the fractional multi-modulus prescaler utilizing the polyphase filter as disclosed and claimed in the present invention.

Further, the difference between prescalers utilizing the M/S half speed circuit means of Craninckx and the polyphase filter of the invention is the readily apparent when both prescaler topologies are compared wherein the frequency of the input signal is the same for both topologies. A phase selector following the M/S half speed circuit means of the Craninckx dual-modulus prescaler sees half the frequency of the input signal. In contrast, a phase selector following a polyphase filter sees the same frequency as the input signal in Applicant's multi-modulus prescaler. The cycle time of the halved frequency in the Craninckx prescaler topology is double the cycle time of the input

signal. Depending on the frequency, the phase selector output may see glitches if the cycle time is too long that is, the time between the 90° phase signals is too long. By providing as high a frequency as possible in the input of the phase selector, the possibility of glitches (the multi-modulus prescaler generation of spurious frequencies) is eliminated in accordance with the invention and thus provides a solution to the problem of spurious frequency generation utilizing prescaler topologies such as the M/S half speed circuit means disclosed in Craninckx.

Claim Rejections 35 U.S.C. §102

The Examiner rejects claims 1-13 as being anticipated by the Craninckx et al. IEEE Journal Publication for the reasoning set forth in paragraph 4 of the Office Action. The Examiner argues Craninckx et al. teaches all the structural limitations of the claimed invention *ex parte Masham*, 2 USPQ2d 1647 (1987) as the basis for the rejection. Even if the Craninckx et al. prior art device performs all the functions recited in the claim as asserted by the Examiner, the prior art cannot anticipate the claim if there is any structural difference. *In re Robertson*, 49 USPQ2d 1949 (Fed. Cir. 1999). It is well settled a single prior art reference anticipates a patent claim if it expressly or inherently describes each and every limitation set forth in the patent claim. *Verdegaal Bros., Inc., v. Union Oil Co.*, 2 USPQ2d 1051 (Fed. Cir. 1987). Inherent anticipation requires that the missing descriptive material is "necessarily present," not merely, probably or possibly present, in the prior art. *Trintec Industries, Inc. v. Top-U.S.A. Corp.* 63 USPQ2d 1597,

CAFC 2002. Applicant respectfully disagrees with the rejection of the claims as being anticipated by Craninckx et al. for the following cogent reasons.

Applicant's invention provides a fractional multi-modulus prescaler without modulus caused spurious frequencies wherein the fractional multi-modulus prescaler operates directly on the input frequency signal which is input to a polyphase filter. Although it is an inherent property of a polyphase filter that the frequency of the output signal is the same frequency of the input signal to the polyphase filter and is well known and understood by those skilled in the art, claim 1 is amended to recite the limitation that the output phase signals have the same frequency as the polyphase input frequency signal. Support for the amendment is found at page 4, lines 30-32 and elsewhere in the specification. No new issues or subject matter is presented by way of the amendment as the amendment merely recites an inherent property of the polyphase filter.

The objective of the Craninckx dual-modulus prescaler as stated at page 891, first column is to reduce the power consumption and to decrease the input frequency by using the M/S half speed circuit.

Craninckx states at column 1, second paragraph, page 891 that the new dual-modulus prescaler topology proposed consists of a pure divide-by-two circuit interrupted by a phase-select block. Since the frequency limiting first stage is only one toggle flip-flop, input frequencies as high as asynchronous dividers can be obtained. The dual-modulus operation is based on the 90° phase relationship between the outputs of the master and the slave of a Master/Slave (M/S) D-flip-flop. Accordingly, Craninckx

teaches and argues that the M/S half speed circuit must be an M/S toggle flip-flop to achieve the reduction in the power consumption and decrease the input frequency.

There is no teaching or suggestion or motivation to replace the M/S half speed circuit means in Craninckx with a polyphase filter because the polyphase would not work in the Craninckx circuit and would not fulfill the objective of achieving lower power consumption and a lower input frequency since the frequency of the polyphase filter output signal is the same as the frequency of the input signal to the polyphase filter. Therefore, Craninckx does not perform all of the functions recited in Applicant's independent claims 1, 9 and 13.

Craninckx further expressly states at page 893, first column, that the second divide-by-two circuit must be an M/S toggle flip-flop. Its design is based on the first divider, but the bias current source is not omitted. This is necessary to cope with the smaller input amplitude and the higher DC level of its input signal which is the output signal of the first divider-by-two. Since this divider operates at half the output frequency, the speed enhancement which resulted from omitting the bias current is no longer necessary. The current output amplitude is 0.5 volts peak-to-peak.

Accordingly, Craninckx teaches that a divide-by-two circuit is absolutely necessary to achieve its goal and objective and to operate to provide the dual-modulus prescaler. Therefore, a polyphase filter as disclosed and claimed in Applicant's invention cannot replace the M/S half speed circuit of Craninckx because Craninckx would be rendered inoperative to achieve its stated goal. Likewise the substitution of the M/S half

speed circuit of Craninckx in Applicant's invention would render Applicant's fractional mutli-modulus prescaler inoperative to achieve its intended goal and would result in longer cycle times resulting in the generation of modulus generated spurious frequencies. Therefore, Craninckx does not teach all of the structured limitations of Applicants claimed invention.

The Examiner asserts that a phase select circuit means is equivalent to a multiplexer and is connected to the M/S half speed circuit for selecting one or more phase signals based on one or more control signals, referencing particularly Figure 7 and page 893, right column, lines 6-7 and 8-17. Craninckx teaches that the phase select circuitry shown in Fig. 7 is a two stage process in which in the first stage both the in-phase and the quadrature signals are amplified in a differential-to-single-ended amplifier and that the amplifier is switched between positive and negative amplification thereby making a selection between the positive signals or the negative signals. The control signals C1 and C2 are used for this selection.

There is no teaching, disclosure or suggestion that the phase select circuitry of Craninckx multiplexes the input signal frequency as disclosed and claimed in Applicant's invention in which the multiplexer is connected to the polyphase filter wherein the frequency of the output phase signals is the same frequency as the input signal to the polyphase filter. In Craninckx, the phase select circuitry is connected to the divide-by-two M/S half speed circuit to select between positive signals and negative signals. Accordingly, Applicant submits that Craninckx does not teach, disclose or suggest the

structural limitation of a multiplexer of the Applicant's invention as disclosed and claimed.

Applicant submits that Craninckx does not contain all of the elements of claim 1 and in particular lacks at least "a polyphase filter having an input for receiving an input frequency signal and for producing one more output phase signals each of said one or more output phase signals having the same frequency as the polyphase filter input frequency signal and a phase difference of 90° relative to one another," and further lacks "a multiplexer coupled to said polyphase filter for selecting said one or more output phase signals in response to a multiplexer control signal."

Regarding claims 2-8, these claims depend directly or indirectly upon independent claim 1 and it is submitted that they likewise are not anticipated by the Craninckx et al. reference for similar reasoning in that Craninckx fails to teach, suggest or disclose "a polyphase filter having an input for receiving an input frequency signal and for producing one or more output phase signals each of said one or more output phase signals having the same frequency as the polyphase filter input frequency signal and a phase difference of 90 degrees relative to one another," and further for lacking "a multiplexer coupled to said polyphase filter for selecting said one or more output phase signals in response to a multiplexer control signal" and further for the additional limitations clearly set forth in the dependent claims 2-8.

Independent claim 9 is amended as set forth above and recites a "fractional multi-modulus prescaler for use in a phase locked loop fractional-N frequency synthesizer

comprising means for providing a quadrature signal from the frequency synthesizer output frequency signal having the same frequency as the frequency synthesizer output frequency signal; means for selecting at least one phase signal of said quadrature signal in accordance with a phase select control signal corresponding to the number of the modulus; means for applying a division function to the selected phase signal of said quadrature signal for each of the phase signals selected during a modulus time period, said modulus time period being defined as starting from an original selected phase signal and returning to the original selected phase signal; and means for returning said phase selecting means to the original selected phase prior to said phase selecting means responding to a subsequent phase select control signal, whereby the generation of multi-modulus spurious frequency signals is prevented."

Craninckx does not teach, disclose or suggest "means for providing a quadrature signal from the frequency synthesizer output frequency signal having the same frequency as the frequency synthesizer output frequency signal." Accordingly, Craninckx lacks at least this structural limitation of the claimed invention. Accordingly, Craninckx does not expressly or inherently describe each and every limitation set forth in the patent claim and, as demonstrated above, does not and cannot prevent the generation of multi-modulus spurious frequency signals.

Claim 10 is dependent upon independent claim 9 and is amended as set forth above to provide the proper antecedent basis for a selected phase signal of said quadrature signal.

Claims 11 and 12 recite respectively that the phase selecting means selects two phases of the quadrature signal or four phases of the quadrature signal to provide a dual-modulus prescaler or a four-modulus prescaler, respectively. It is brought to the Examiner's attention that Craninckx is limited to a dual-modulus prescaler architecture and does not teach, disclose or suggest a multi-modulus prescaler as disclosed and described in the present invention. Craninckx is inoperative as a four-modulus prescaler.

Claim 13 is amended as set forth above and recites a "method for providing a spurious frequency-free multi-modulus prescaler comprising providing a quadrature signal corresponding to the output frequency signal of a voltage-controlled oscillator in a phase locked loop fractional-N frequency synthesizer and having the same frequency as the output frequency signal of the voltage-controlled oscillator; selecting one or more phases of the quadrature signal in accordance with a phase select control signal corresponding to the number of the modulus; applying a division function to the selected phase of the quadrature signal for each of the phases selected during a modulus time period to generate the desired fractional multiple of the input reference frequency; and returning to an original selected phase of the quadrature signal prior to responding to a subsequent phase select control signal whereby the generation of multi-modulus spurious frequency signals is prevented."

Cranickx fails to teach, disclose or suggest providing "a quadrature signal corresponding to the output frequency signal of a voltage-controlled oscillator in a phase locked loop fractional-N frequency synthesizer having the same frequency as the output

frequency signal of the voltage-controlled oscillator." Accordingly, Cranickx is deficient with respect to at least this structured limitation of independent claim 13 and therefore cannot anticipate applicant's invention for at least the reasoning set forth above.

Independent claims 9 and 13 further recite the structural limitation that the fractional multi modulus prescaler does not respond to a subsequent frequency control signal without first returning to an original selected phase of the quadrature signal so that the generation of multi modulus spurious frequency signals is prevented. Craninckx et al. is also deficient with respect to this structural limitation in addition to the structural limitations of the claimed invention as identified above.

Regarding the rejection of claims 4, 5, and 6, the Examiner has not shown or explained how the control signals of Cranickx et al. operate to anticipate the structural limitations of Applicant's claimed invention nor is such operation readily apparent from a reading of the reference.

In summary, Applicant submits that the present invention as disclosed and claimed is not anticipated by the Craninckx et al. reference for at least the above reasoning. Craninckx does not teach, disclose or suggest "a polyphase filter to generate phase difference signals that are input to a multiplexer for selection by the phase control in accordance with the phase control input signal generated by the D-CTRL signal and the MOD signal wherein the frequency of the phase difference signals is the same as the frequency of an input signal to the polyphase filter." Applicant further submits that

Craninckx does not teach, suggest or disclose a fractional multi-modulus prescaler as disclosed and claimed.

Accordingly, it is submitted that the present invention as disclosed and claimed is readily distinguishable from the prior art for the reasons indicated. Applicant's invention is not disclosed by any of the prior art and there is no fair basis that Applicant's invention is obvious or anticipated in regard to such prior art. If the invention was obvious, it would have been adopted before in view of its advantages.

Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that all of the claims of the application are allowable and early favorable action is earnestly solicited. The Examiner is invited to call Applicant's attorney if any questions remain following review of this response.

The undersigned respectfully submits that no fee is due for filing this response. The Commissioner is hereby authorized to charge to deposit account 23-0442 any fee deficiency required to submit this paper.

Respectfully submitted,

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